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EXAMINER	
LEE, CHUN KUAN	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,608	RENICK, KIRSTEN	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
7/14/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to because in Figure 3, packets associated with the transaction T4 is not shown on the right side of the figure, prior to be entered into the data organization unit. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 21 is objected to because of the following informalities:

in claim 21, "vary the number of lanes in each lane groups" should be replaced with -vary the number of sub-groups in each groups-. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4, 6, 10-15, 17, 21-25, 28-32, 34, and 38-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Caldara et al. (US Patent 5,748,629).

5. As per claims 1 and 29, AAPA teaches a processor-based system, comprising:

a processor (Drawings, Fig. 1, ref. 104) having a processor bus (Drawings, Fig. 1, ref. 106);

a system controller (Drawings, Fig. 1, ref. 110) coupled to the processor bus, the system controller having a peripheral device port (Specification, [006]);

at least one input device (Drawings, Fig. 1. ref. 118) coupled to the peripheral device port of the system controller (Specification, [006]);

at least one output device (Drawings, Fig. 1. ref. 120) coupled to the peripheral device port of the system controller (Specification, [006]);

at least one data storage device (Drawings, Fig. 1. ref. 124) coupled to the peripheral device port of the system controller (Specification, [006]); and

a memory hub controller (Drawings, Fig. 1, ref. 128) coupled to the processor bus;

a plurality of memory modules (Drawings, Fig. 1, ref. 130a-130n) coupled to the memory hub controller by at least one bus (Drawings, Fig. 1, ref. 134), each of the memory modules comprising:

a plurality of memory devices (Drawings, Fig. 1, ref. 148); and

a memory hub (Drawings, Fig. 1, ref. 140), comprising:

a memory controller coupled to the memory devices (Specification, [007]-[0011]), as the received request for data from the memory modules (Drawings, Fig. 1, ref. 130a-130n) must properly identified in order to be routed to the appropriate memory module and the requested data must

then be properly returned to the memory hub controller (Drawings, Fig. 1, ref. 128), the memory hub must have the memory controller for implementing such routing control;

at least one receive interface coupled to the memory controller through a bus system (Specification, [007]-[011]), in order to receive the memory request to the memory module, the memory hub must have the interface for receiving the memory request through the bus system; and

at least one transmit interface coupled to the memory controller through the bus system to transmit memory transactions from the memory module to the memory controller (Specification, [007]-[011]), in order to transfer the requested data back, resulted from the memory request, there must be the interface for transmitting the requested data to the next memory controller inside the next memory hub or back to the memory controller hub (Drawings, Fig. 1, ref. 128), depending on where the memory module is located (Specification, [009]),

each transmit interface receiving memory transactions each of which comprises a command header and data having a variable number of data bits (Drawings, Fig. 2, ref. 162, 164, 166, 168 and Specification, [012]), wherein the number of data bits depends on the number of 32-bit groups of data,

each transmit interface including a data organization system (Drawings, Fig. 2) organizing the command header and data into

lane groups (Drawings, Fig. 2, ref. 175-179) each of which includes a plurality of lanes (i.e. eight lanes) each of which contains a plurality of parallel command header bits or parallel data bits (Drawings, Fig. 2, ref. 175-179 and Specification, [012]),

the data organization system (Drawings, Fig. 2) being operable to convert each of the lane groups into a serial stream of the lanes for transmission by the transmit interface (Drawings, Fig. 2, ref. 174), wherein parallel data are serially outputted (Drawings, Fig. 2, ref. 134) , as the conversion is implemented by the parallel to serial converter (Drawings, Fig. 2, ref. 174),

each of the transmitted lanes containing a plurality of parallel command header bits or parallel data bits (Drawings, Fig. 2, ref. 134 and Specification, [012]).

AAPA does not expressly teach the data organization system organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits.

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and transferring the buffered data cells without processing any empty storage location, as available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 5-10 and col. 3, ll.28-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Caldara's buffering the current data cell right after the previously buffered data cell without leaving any empty buffer location into AAPA's data organization system. The resulting combination of the references teaches the processor-based system comprising wherein the data organization system fill all the lanes (i.e. buffers) by buffering the current data cell right after the previously buffered data cell without leaving any empty buffer location, therefore buffering either command header bits or data bits.

Therefore, it would have been obvious to combine Caldara with AAPA for the benefit of implementing data transferring system that is able to dynamically accommodate for changes in the data traffic and bandwidth requirements (Caldara, col. 1, ll. 57-60).

6. As per claims 2 and 30, AAPA and Caldara teach all the limitations of claims 1 and 29 as discussed above, where AAPA further teaches the processor-based system comprising wherein each of the lane groups comprise eight lanes (AAPA, Drawings, Fig. 2, ref. 175-179).

7. As per claims 3 and 31 AAPA and Caldara teach all the limitations of claims 1 and 29 as discussed above, where AAPA further teaches the processor-based system comprising wherein each of the lanes comprise 32 parallel bits of command header or data (AAPA, Specification, [012]).

8. As per claim 4 and 32, AAPA and Caldara teach all the limitations of claims 1 and 29 as discussed above, where both further teach the processor-based system comprising wherein the bus system comprises:

a downstream bus (AAPA, Drawings, Fig. 1, ref. 134) for coupling memory transactions transmitted by the memory modules away from the memory controller (AAPA, Specification, [009]) and

an upstream bus for coupling memory transactions transmitted by the memory modules toward the memory controller (AAPA, Specification, [009]), and

wherein the transmit interface comprises an upstream transmit interface coupled to the upstream bus and a downstream transmit interface coupled to the downstream bus (AAPA, Specification, [007]-[012] and Caldara, Fig. 1 ref, 20, 22),

each of the upstream and downstream transmit interfaces including a respective one of the data organization systems (Caldara, Fig. 1 ref, 20, 22), wherein each input or output port have the corresponding data processing system.

9. As per claim 6 and 34, AAPA and Caldara teach all the limitations of claims 1 and 29 as discussed above, where both further teach the processor-based system comprising wherein the data organization system comprises:

a data organization unit (AAPA, Drawings, Fig. 2, ref. 160) organizing the command header and data into lane groups each of which includes a plurality of lanes containing either a command header or data (AAPA, Drawings, Fig. 2, ref. 175-179), the

data organization unit organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits (Caldara, Fig. 6; col. 3, ll. 4-9 and col. 3, ll.28-33); and

a parallel-to-serial converter (AAPA, Drawings, Fig. 2, ref. 174) converting each of the lane groups into a serial stream of the lanes for transmission by the transmit interface (AAPA, Specification, [012]).

10. As per claims 10 and 38, AAPA and Caldara teach all the limitations of claims 1 and 34 as discussed above, where both further teach the processor-based system comprising wherein the data organization system comprises wherein the data organization unit is configurable to vary the number of lanes in each lane groups that are coupled from the data organization during each cycle of a clock signal (AAPA, Specification, [010] and Caldara, col. 6, ll. 11-17), as the bandwidth can be dynamically reallocated, therefore the number of lanes can be configured to be varied.

11. As per claims 11 and 39, AAPA and Caldara teach all the limitations of claims 1 and 29 as discussed above, where AAPA further teaches the processor-based system comprising wherein the command header and data for each of the transactions comprise a memory packet (AAPA, Specification, [008]).

12. As per claim 12, AAPA teaches a memory module, comprising:

a plurality of memory devices (Drawings, Fig. 1, ref. 148); and

a memory hub (Drawings, Fig. 1, ref. 140), comprising:

a memory controller coupled to the memory devices (Specification, [007]-[0011]), as the received request for data from the memory modules (Drawings, Fig. 1, ref. 130a-130n) must properly identified in order to be routed to the appropriate memory module and the requested data must then be properly returned to the memory hub controller (Drawings, Fig. 1, ref. 128), the memory hub must have the memory controller for implementing such routing control;

at least one receive interface coupled to the memory controller (Specification, [007]-[011]), in order to receive the memory request to the memory module, the memory hub must have the interface for receiving the memory request through the bus system; and

at least one transmit interface coupled to the memory controller to transmit memory transactions from the memory module (Specification, [007]-[011]), in order to transfer the requested data back, resulted from the memory request, there must be the interface for transmitting the requested data to the next memory controller inside the next memory hub or back to the memory controller hub (Drawings, Fig. 1, ref. 128), depending on where the memory module is located (Specification, [009]),

each transmit interface receiving memory transactions each of which comprises a command header and data having a variable number of data bits (Drawings, Fig. 2, ref. 162, 164, 166, 168 and Specification,

[012]), wherein the number of data bits depends on the number of 32-bit groups of data,

each transmit interface including a data organization system (Drawings, Fig. 2) that is operable to organize the command header and data into groups (Drawings, Fig. 2, ref. 175-179) each of which contains a predetermined number of sub-groups (i.e. eight sub-groups) of a predetermined size (i.e. 32-bits) (Drawings, Fig. 2, ref. 175-179 and Specification, [012]),

each of the sub-groups containing a plurality of parallel command header bits or data bits (Drawings, Fig. 2, ref. 134 and Specification, [012]),

the data organization system further being operable to output each group of data as a serial stream of the sub-groups (Drawings, Fig. 2, ref. 134), as parallel data is converted to serial data by the parallel to serial data converter (Drawings, Fig. 2, ref. 174).

AAPA does note expressly teach that each sub-group containing data for a first transaction being immediately followed by a sub-group containing either additional data for the first transaction or the command header for a second transaction so that each group is filled with sub-groups containing either command header bits or data bits,

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and

transferring the buffered data cells without processing any empty storage location, as available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 4-9 and col. 3, ll.28-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Caldara's the storing of data cells without leaving any empty storage cells between the previously stored data cell and the currently stored data cell into AAPA's memory module.

Therefore, it would have been obvious to combine Caldara with AAPA for reason stated above in claims 1 and 29.

13. As per claim 13, AAPA and Caldara teach all the limitations of claim 12 as discussed above, where AAPA further teaches the memory module comprising wherein each of the groups comprise eight sub-groups (AAPA, Drawings, Fig. 2, ref. 175-179).

14. As per claim 14, AAPA and Caldara teach all the limitations of claim 12 as discussed above, where AAPA further teaches the memory module comprising wherein each of the sub-groups comprise 32 parallel bits of command header or data (AAPA, Specification, [012]).

15. As per claim 15, AAPA and Caldara teach all the limitations of claim 12 as discussed above, where both further teach the memory module comprising wherein the at least one transmit interface comprises an upstream transmit interface and a

downstream transmit interface (AAPA, Specification, [007]-[012] and Caldara, Fig. 1 ref, 20, 22) each of which comprises the data organization system (Caldara, Fig. 1 ref, 20, 22), wherein each input or output port have the corresponding data processing system.

16. As per claim 17, AAPA and Caldara teach all the limitations of claim 12 as discussed above, where both further teach the memory module comprising:

a data organization unit (AAPA, Drawings, Fig. 2, ref. 160) organizing the command header and data into groups each of which includes a plurality of the sub-groups containing either a command header or data (AAPA, Drawings, Fig. 2, ref. 175-179), the data organization unit organizing the groups so that all of the sub-groups in each group are filled with either command header bits or data bits (Caldara, Fig. 6; col. 3, ll. 4-9 and col. 3, ll.28-33); and

a parallel-to-serial converter (AAPA, Drawings, Fig. 2, ref. 174) converting each of the groups into a serial stream of the sub-groups for transmission by the transmit interface (AAPA, Specification, [012]).

17. As per claim 21, AAPA and Caldara teach all the limitations of claim 17 as discussed above, where both further teach the memory module comprising wherein the data organization unit is configurable to vary the number of sub-groups in each groups that are coupled from the data organization during each cycle of a clock signal (AAPA, Specification, [010] and Caldara, col. 6, ll. 11-17), as the bandwidth can be dynamically reallocated, therefore the number of lanes can be configured to be varied.

18. As per claim 22, AAPA and Caldara teach all the limitations of claim 12 as discussed above, where AAPA further teaches the memory module comprising wherein the command header and data for each of the transactions comprise a memory packet (AAPA, Specification, [008]).

19. As per claim 23, AAPA teaches a data organization system (Fig. 2), comprising:

a data organization unit (Drawings, Fig. 2, ref. 160) organizing a command header and data for each of a plurality of memory transaction into lane groups each of which includes a plurality of lanes each of which contains a plurality of parallel command header bits or parallel data bits (Drawings, Fig. 2, ref. 175-179 and Specification, [012]); and

a parallel-to-serial converter (Drawings, Fig. 2, ref. 174) converting each of the lane groups into a serial stream of the lanes each of which contains a plurality of parallel command header bits or parallel data bits (AAPA, Specification, [012]).

AAPA does not teach the data organization system comprising wherein the data organization unit organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and transferring the buffered data cells without processing any empty storage location, as

available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 4-9 and col. 3, ll.28-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Caldara's the storing of data cells without leaving any empty storage cells between the previously stored data cell and the currently stored data cell into AAPA's data organization system.

Therefore, it would have been obvious to combine Caldara with AAPA for reason stated above in claims 1 and 29.

20. As per claim 24, AAPA and Caldara teach all the limitations of claim 23 as discussed above, where AAPA further teaches the data organization system comprising wherein each of the lane groups comprise eight lanes (AAPA, Drawings, Fig. 2, ref. 175-179).

21. As per claim 25, AAPA and Caldara teach all the limitations of claim 23 as discussed above, where AAPA further teaches the data organization system comprising wherein each of the lanes comprise 32 parallel bits of command header or data (AAPA, Specification, [012]).

22. As per claim 28, AAPA and Caldara teach all the limitations of claim 23 as discussed above, where both further teach the data organization system comprising wherein the data organization unit is configurable to vary the number of lanes in each

lane groups that are coupled from the data organization during each cycle of a clock signal (AAPA, Specification, [010] and Caldara, col. 6, ll. 11-17), as the bandwidth can be dynamically reallocated, therefore the number of lanes can be configured to be varied.

23. As per claim 40, AAPA teaches a method of transmitting memory transactions each of which comprises a command header and a variable amount of data (Drawings, Fig. 2 ref. 162-168), the method comprising:

organizing the command header and data into groups each of which contains a predetermined number of sub-groups (i.e. eight sub-groups) of a predetermined size (i.e. 32-bit) (Drawings, Fig. 2 and Specification, [010]-[011]),

each of the sub-groups containing a plurality of parallel command header bits or data bits (Specification, [012]); and

transmitting each group of data as a serial stream of the sub-groups (Drawings, Fig. 2, ref. 134) each of which includes the plurality of parallel command header bits or data bits (Specification, [012]), as parallel data is converted to serial data by the parallel to serial data converter (Drawings, Fig. 2, ref. 174).

AAPA does not expressly teach the method comprising wherein each sub-group containing data for a first transaction being immediately followed by a sub-group containing either additional data for the first transaction or the command header for a second transaction so that each group is filled with sub-groups containing either command header bits or data bits.

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and transferring the buffered data cells without processing any empty storage location, as available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 4-9 and col. 3, ll.28-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Caldara's the storing of data cells without leaving any empty storage cells between the previously stored data cell and the currently stored data cell into AAPA's method of transmitting memory transactions.

Therefore, it would have been obvious to combine Caldara with AAPA for reason stated above in claims 1 and 29.

24. As per claim 41, AAPA and Caldara teach all the limitations of claim 40 as discussed above, where AAPA further teaches the method comprising wherein the act of organizing the command header and data into groups comprises organizing the command header and data into groups each of which contains eight sub-groups (AAPA, Drawings, Fig. 2, ref. 175-179).

25. As per claim 42, AAPA and Caldara teach all the limitations of claim 40 as discussed above, where AAPA further teaches the method comprising wherein the act of organizing the command header and data into groups containing a predetermined

number of sub-groups comprises the command header and data so that each sub-group comprises 32 parallel bits of command header or data (AAPA, Specification, [012]).

26. As per claim 43, AAPA and Caldara teach all the limitations of claim 40 as discussed above, where Caldara further teaches the method further comprising varying the quantity of sub-groups in each group (Caldara, col. 6, ll. 11-17), as the bandwidth can be dynamically reallocated, therefore the number of sub-groups can be configured to be varied.

27. As per claim 44, AAPA teaches a method of transmitting memory transactions each of which comprises a command header and a variable amount of data (Drawings, Fig. 2, ref. 162-168), the method comprising:

organizing the command header and data into lane groups (Drawings, Fig. 2, ref. 175-179) each of which contains a plurality of lanes of a predetermined size (i.e. eight lanes) (Drawings, Fig. 2, ref. 175-179),

each of the lanes containing a plurality of parallel command header bits or data bits (Specification, [012]).

AAPA does not expressly teach the method comprising wherein the lane groups being organizing so that all of the lanes in each lane group are filled with either command header bits or data bits.

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and transferring the buffered data cells without processing any empty storage location, as available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 4-9 and col. 3, ll.28-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Caldara's the storing of data cells without leaving any empty storage cells between the previously stored data cell and the currently stored data cell into AAPA's method of transmitting memory transactions.

Therefore, it would have been obvious to combine Caldara with AAPA for reason stated above in claims 1 and 29.

28. As per claim 45, AAPA and Caldara teach all the limitations of claim 44 as discussed above, where AAPA further teaches the method further comprising converting each of the lane groups into a serial stream of the lanes (AAPA, Drawings, Fig. 2, ref. 134) each of which contains a plurality of parallel command header bits or parallel data bits (AAPA, Specification, [012]).

29. As per claim 46, AAPA and Caldara teach all the limitations of claim 44 as discussed above, where AAPA further teaches the method comprising wherein the act of organizing the command header and data into lane groups comprises organizing the

command header and data into lane groups each of which contains eight lanes (AAPA, Drawings, Fig. 2, ref. 175-179).

30. As per claim 47, AAPA and Caldara teach all the limitations of claim 44 as discussed above, where AAPA further teaches the method comprising wherein the act of organizing the command header and data into lane groups each of which contains a predetermined number of lanes comprises organizing the command header and data so that each lane comprises 32 parallel bits of command header or data (AAPA, Specification, [012]).

31. As per claim 48, AAPA and Caldara teach all the limitations of claim 44 as discussed above, where AAPA further teaches the method further comprising varying the number of lanes in each lane group (Caldara, col. 6, ll. 11-17), as the bandwidth can be dynamically reallocated, therefore the number of sub-groups can be configured to be varied.

32. Claims 5, 7-9, 16, 18-20, 26-27, 33 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) and Caldara et al. (US Patent 5,748,629), and in view of Epps et al. (US Patent (6,778,546).

33. As per claims 5, 7, 33 and 35, AAPA and Caldara teach all the limitation of claim 1, 6, 29 and 34 as discussed above.

AAPA and Caldara does not expressly teach the processor-based system comprising:

wherein the memory devices comprise dynamic random access memory devices;

wherein the data organization unit comprises:

a data buffer storing respective data for a plurality of the transactions, the data for each of the transactions being selectively passed from the data buffer; and

a command queue storing respective command headers for a plurality of the transactions, the command header for each of the transactions being selectively passed from the command queue with the data for the corresponding transaction being passed from the data buffer.

Epps teaches a system and a method comprising:

a memory device comprising a SDRAM (col. 25, ll. 46-51), wherein the SDRAM is a type of DRAM (dynamic random access memory);

a header queue (Fig. 3, ref. 320), buffering the header of the data block (col. 6, ll. 1-12);

a tail queue (Fig. 3, ref. 330), buffering the tail of the data block (col. 6, ll. 1-12); and

wherein the header and tail are selectively transferred through a switch (Fig. 2-3 ref. 220; Fig. 3, ref. 470 and col. 7, ll. 13-20).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Epps' SDRAM, header buffer and tail buffer into AAPA

and Caldara's processor-based system. The resulting combination of the references teaches processor-based system further comprising:

the memory devices comprise SDRAM;

the header queue buffering the command headers;

the tail queue buffering the data; and

wherein the command header and the data are selectively transferred from the queues by the switch.

Therefore, it would have been obvious to combine Epps with AAPA and Caldara for the benefit of providing a flexible transferring system with ultra-high throughput (Epps, col. 3, ll. 1-10).

34. As per claims 8 and 36, AAPA, Caldara and Epps teach all the limitations of claims 7 and 35 as discussed above, where Caldara and Epps further teach the processor-based system comprising:

a multiplexer (Epps, Fig. 3, ref. 470) coupled to receive the data stored in the data buffer (Epps, Fig. 3, ref. 330) for each of the transactions and the command headers stored in the command queue (Epps, Fig. 3, ref. 320) for each of the transactions, the multiplexer being operable to couple the data for each of the transactions and the command header for each of the transactions to an output port responsive to multiplexer control signals (Epps, Fig. 11; col. 7, ll. 13-20 and col. 15, ll. 8-21), wherein the multiplexer control signals is provided by the MUX control block in the Transfer MUX block (Epps, Fig. 11, ref. 470);

an arbitration unit (Caldara, To Switch Port Processor (TSPP) Fig. 6 and Epps, the MUX control block in the Transfer MUX block 470 of Fig. 11) coupled to at least one of the data buffer and the command queue to receive information indicative of the data and command headers for the transactions stored in the data buffer and command queue (Caldara, col. 2, ll. 57-67), as priority associated with the data is received, respectively, the arbitration unit being operable to generate the control signals responsive to the information indicative of the data and command headers to cause the multiplexer to couple a lane group of either data or a command header and data for at least one of the transactions to the output port of the multiplexer (Fig. 11), as the MUX Control provide the control signal, base on the priority of the data, informing the multiplexer which buffered data cells to output.

35. As per claims 9 and 37, AAPA, Caldara and Epps teach all the limitations of claims 8 and 36 as discussed above, where AAPA further teaches the processor-based system further comprising:

a parallel-to-serial converter (AAPA, Drawings, Fig. 2, ref. 174) coupled to the output port of the multiplexer, the parallel-to-serial converter being operative to convert the lane group at the output port of the multiplexer into a serial stream of the lanes (AAPA, Drawings, Fig. 2, ref. 134 and Specification, [012]).

36. Claims 16 and 18-20 repeat the limitations of claims 5 and 7-9 and are therefore rejected accordingly.

37. Claims 26-27 repeat the limitations of claims 7-8 and are therefore rejected accordingly.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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C.K.L.
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